AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) A method for synchronizing a clock signal to a data signal, comprising the steps of:

(A) detecting an edge of said data signal;

(B) generating a numeric representation of a magnitude of a phase error between (i) said edge of said data signal and (ii) said clock signal;

~~(B)~~ (C) determining whether said numeric representation ~~a position of said edge~~ is within a predetermined zone; ~~and~~

~~(B)~~ (D) if said ~~edge~~ numeric representation is not within said predetermined zone, adjusting said clock signal towards said position of said edge; and

(E) if said numeric representation is within said predetermined zone, repeating steps (A)-(C).

2. (ORIGINAL) The method of claim 1, wherein step (A) comprises the sub-step of:

(A-1) sampling a number of clock signals using said data signal.

3. (ORIGINAL) The method according to claim 2, wherein step (A) further comprises the sub-step of:

(A-2) encoding a position of said edge.

4. (ORIGINAL) The method of claim 1, wherein step (B) further comprises:

comparing an encoded position of said edge to a predetermined value.

5. (ORIGINAL) The method of claim 3, wherein step (A) further comprises the sub-step of:

storing said encoded position.

6. (CURRENTLY AMENDED) The method of claim 1, wherein step (C) comprises the sub-step of:

incrementing ~~a~~ an accumulated value in response to a first polarity.

7. (CURRENTLY AMENDED) The method according to claim 6, wherein step (C) further comprises the sub-step of decrementing said accumulated value in response to a second polarity.

8. (CURRENTLY AMENDED) The method of claim 1, wherein step (C) further comprises the sub-step of selecting a number of clock phases based upon said accumulated value.

9. (CURRENTLY AMENDED) An apparatus for synchronizing a clock signal to a data signal, comprising:

a detector configured to produce a numeric value representing a position of an edge of said data signal based upon a state of said clock signal; and

a control ~~circuitry~~ circuit configured to adjust said clock signal when said position of said edge is not within a predetermined zone, wherein said adjustment comprises adjusting said clock signal towards said position of said edge.

10. (CURRENTLY AMENDED) The apparatus of claim 9, wherein the control circuitry further comprises a storage element configured to store an accumulated value representing an encoded position of said edge.

11. (CURRENTLY AMENDED) The apparatus of claim 9, wherein said control circuitry further comprises an increment/decrement logic circuit configured to adjust ~~a third~~ said accumulated value in response to said numeric value, wherein said accumulated value is updated each time said detector produces said numeric value ~~said second value~~.

12. (ORIGINAL) The apparatus of claim 9, wherein said clock signal comprises a plurality of phases.

13. (ORIGINAL) The apparatus of claim 9, wherein said control circuitry selects one or said plurality of phases as a system clock.

14. (CURRENTLY AMENDED) An apparatus for synchronizing a clock signal to a data signal, comprising:

means for detecting an edge of said data signal;

means for generating a numeric representation of a magnitude of a phase error between (i) said edge of said data signal and (ii) said clock signal;

means for determining whether ~~a position of said edge~~ said numeric representation is within a predetermined zone; ~~and~~

means for adjusting said clock signal towards said position of said edge when said position of said edge is not within said predetermined zone; and

if said numeric representation is within said predetermined zone, repeating steps (A)-(D).

15. (NEW) A method for synchronizing a clock signal to a data signal, comprising the steps of:

(A) detecting an edge of a data signal;

(B) determining a relative polarity and phase offset magnitude as a numeric representation of said edge of said data signal relative to said clock signal;

(C) if said magnitude is less than a predetermined value, repeating steps (A) and (B);

(D) if said magnitude is greater than a predetermined value, determining a polarity of said magnitude.

(E) adjusting said clock (i) counter-clockwise if said polarity is positive and (ii) clockwise if said polarity is not positive.

16. (NEW) The method according to claim 15, further comprising the step of:

generating an accumulated value for said numeric representation of said magnitude, wherein said accumulated value is updated each pass through step (B).